Abstract of the Disclosure

A method for fabrication of silicon-on-nothing (SON) MOSFET using selective etching of $Si_{1-x}Ge_x$ layer, includes preparing a silicon substrate; growing an epitaxial $Si_{1-x}Ge_x$ layer on the silicon substrate; growing an epitaxial thin top silicon layer on the epitaxial $Si_{1-x}Ge_x$ layer; trench etching of the top silicon and $Si_{1-x}Ge_x$, into the silicon substrate to form a first trench; selectively etching the $Si_{1-x}Ge_x$ layer to remove substantially all of the $Si_{1-x}Ge_x$ to form an air gap; depositing a layer of SiO_2 by CVD to fill the first trench; trench etching to from a second trench; selectively etching the remaining $Si_{1-x}Ge_x$ layer; depositing a second layer of SiO_2 by CVD to fill the second trench, thereby decoupling a source, a drain and a channel from the substrate; and completing the structure by state-of-the-art CMOS fabrication techniques.